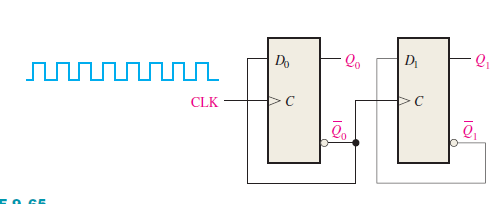
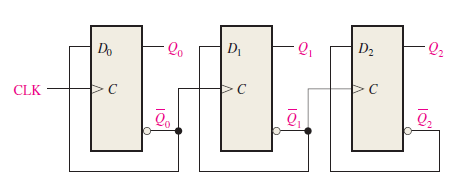
**Chapter-9 (Practice Questions)**

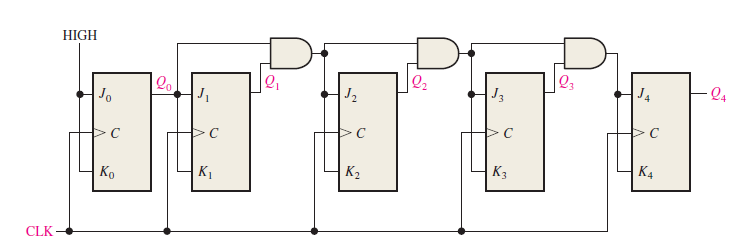
1. For the ripple counter shown in Figure , show the complete timing diagram for eight clock pulses, showing the clock, Q0, and Q1 waveforms.



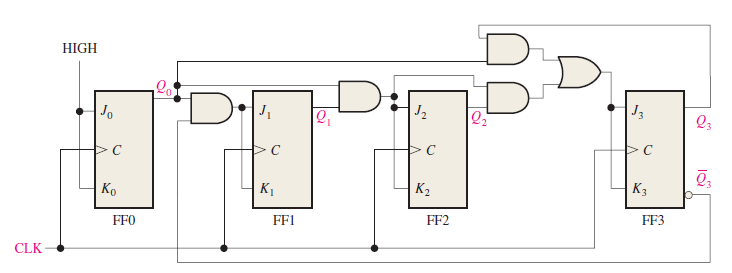
1. For the ripple counter in Figure , show the complete timing diagram for sixteen clock pulses. Show the clock, Q0, Q1, and Q2 waveforms.



1. Show how to connect a 74HC93 4-bit asynchronous counter for each of the following moduli: (a) 9 (b) 11 (c) 13 (d) 14 (e) 15
2. Show the complete timing diagram for the 5-stage synchronous binary counter in Figure. Verify that the waveforms of the Q outputs represent the proper binary number after each clock pulse.



1. By analyzing the J and K inputs to each flip-flop prior to each clock pulse, prove that the decade counter in Figure progresses through a BCD sequence. Explain how these conditions in each case cause the counter to go to the next proper state.



1. The waveforms in Figure are applied to the count enable, clear, and clock inputs as indicated. Show the counter output waveforms in proper relation to these inputs. The clear input is asynchronous.

